System in Package Technologies for Space Applications

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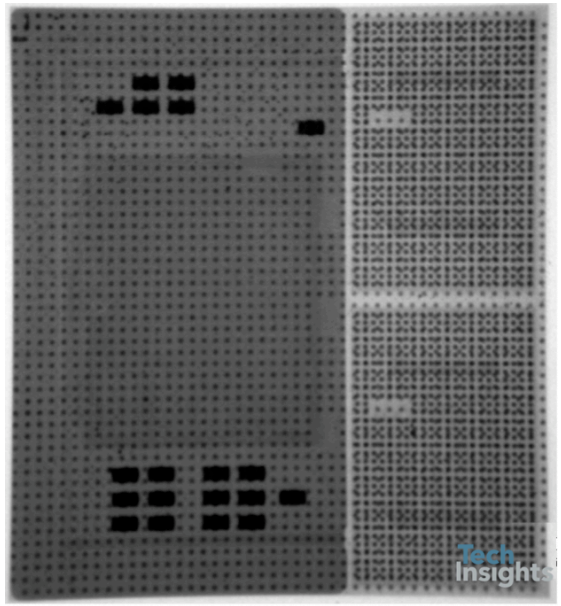
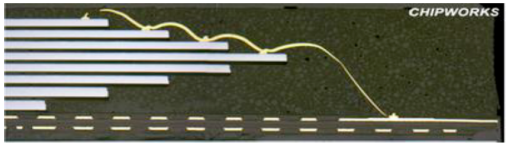
Example of modern packaging

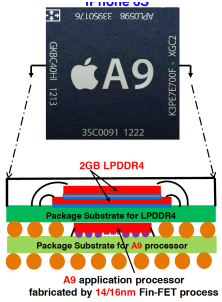


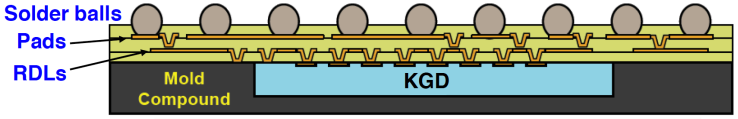
- De-lidded BGA with the die flip-chipped conventionally onto the substrate under a truncated metal top, and the memory FBGAs mounted beside it.
- Dimensional considerations drive continuous innovation
- Power management and performance are optimized by reducing communication paths between chips

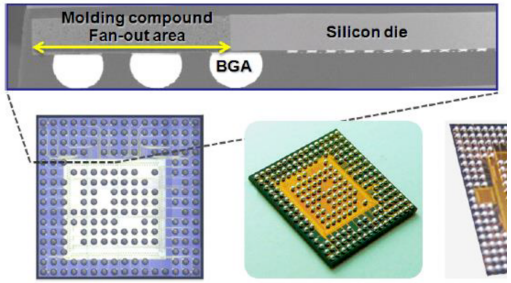
Enormous variation in packaging solutions to meet stringent modern commercial product requirements

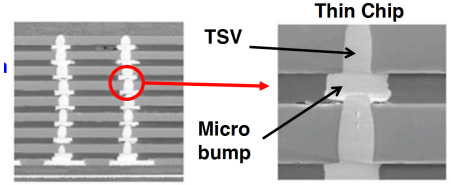
The ever changing world of packaging

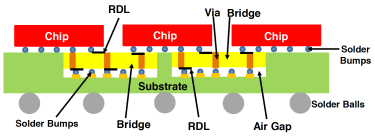


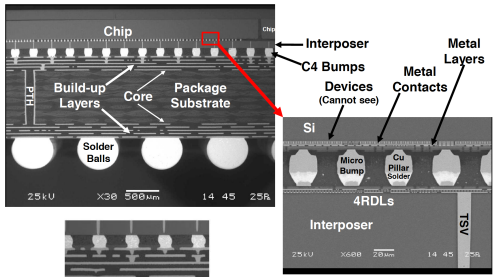


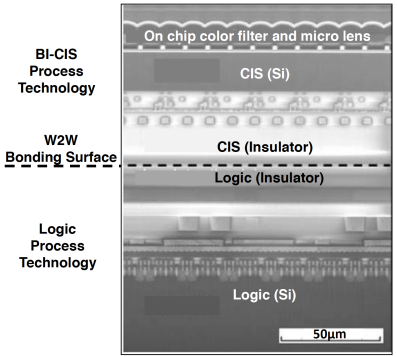


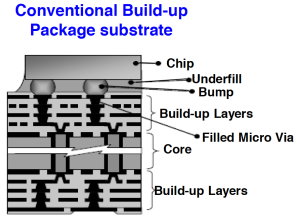


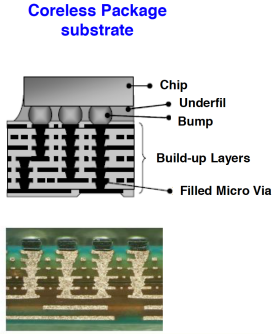




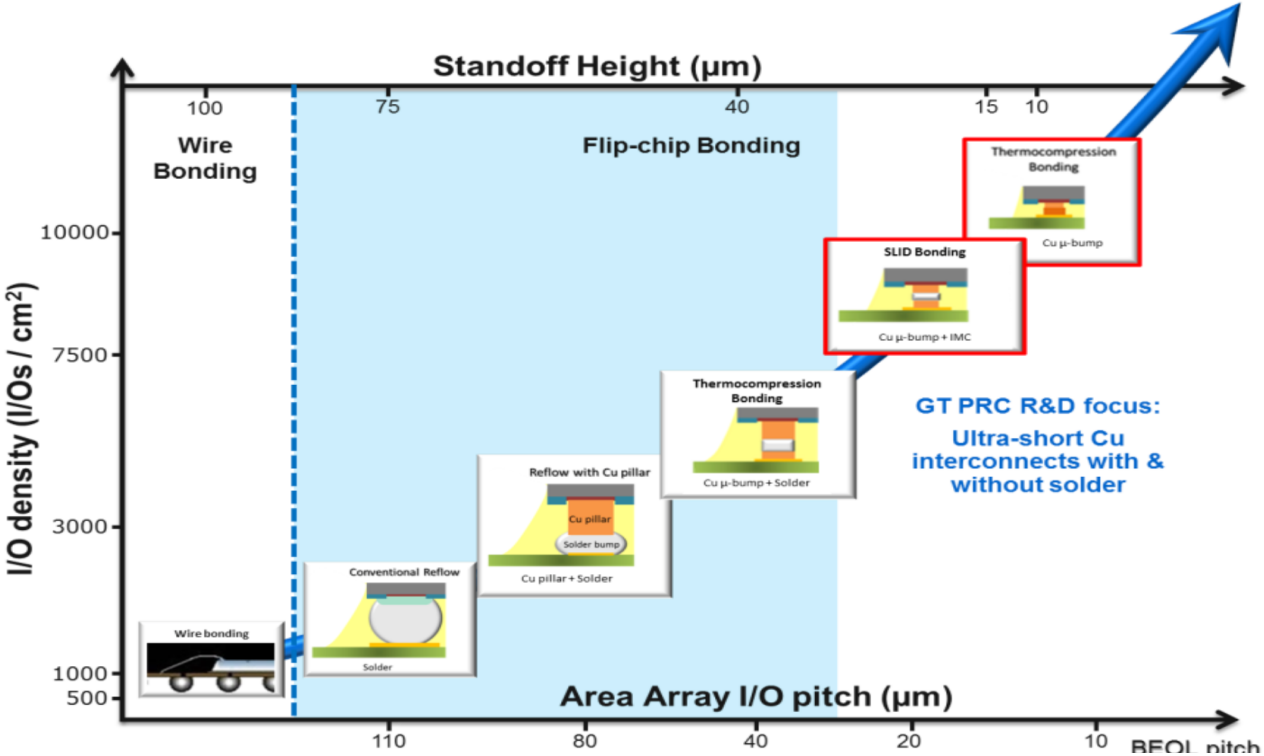






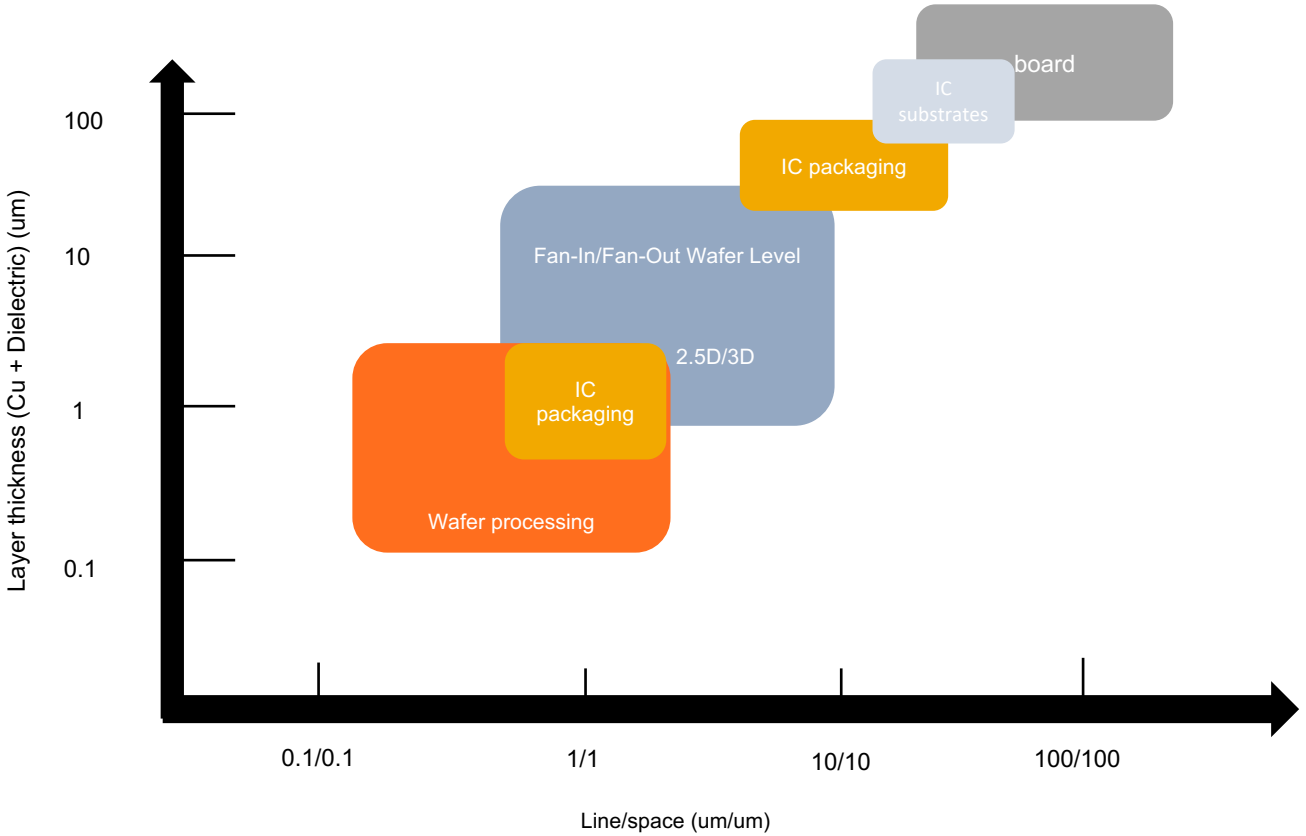


Scaling roadmap – I/O pitch, density and standoff height



Mil-Aero parts are progressing along this roadmap

Substrate Technology Scaling



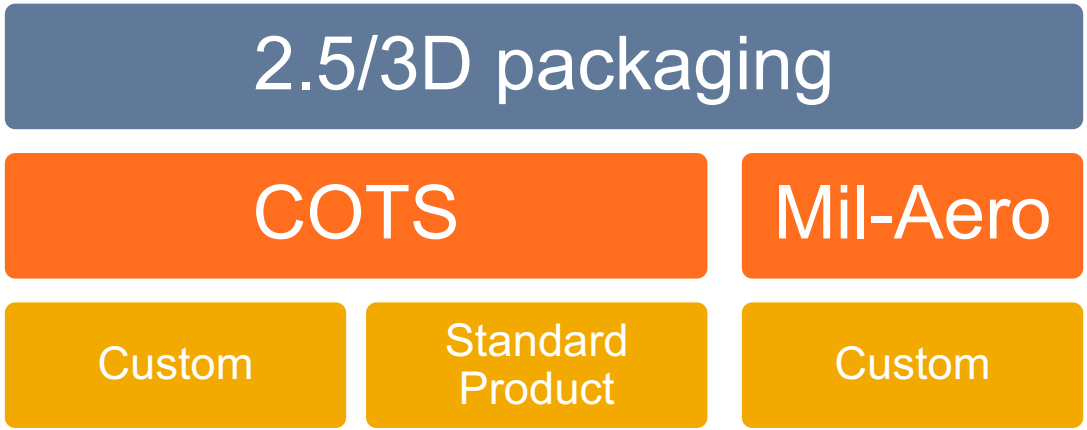
- Historically wafers, IC and boards were separate
- Modern packaging has blurred those boundaries
- Substrate and interposer technologies are the driving force
- Technology pitch (L/S) can be used as a technology reference point
- Different decades of pitch requires a different substrate and attachment technology solution(s).

Comments about space grade SiP technology

- Modern SiP technology is commercial technology
- Commercial technologies are often qualified to the end use condition
- Typical space grade ”standards based” qualification, could over or under predict reliability
- Limiting failure modes in the chip-package-board system maybe very different for different applications.
- Standards based approach doesn’t easily address this

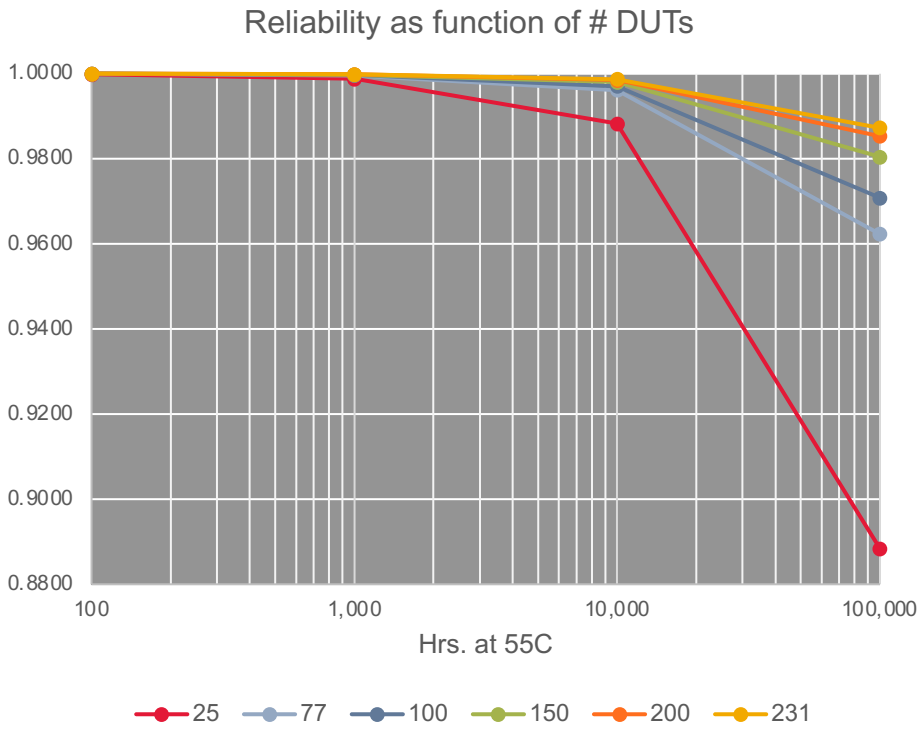
Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
THB(1) or HAST(1)	85°C, 85% RH, V_{DD}	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			
Temperature cycling(1) (2) (3) (4)	–65°C to +150°C	500 cycles	3	25	0 failures
	–55°C to +125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Autoclave(1) or temperature humidity unbiased(1) or HASTU(1)	121°C, 100% RH	96 hours	3	25	0 failures
	85°C, 85% RH	1,000 hours			
	130°C, 85% RH or 110°C, 85% RH	96 hours or 264 hours			
High-Temperature Storage (HTS)	T_A=150°C	1,000 hours	3	25	0 failures

Basic Overview of Packaging Landscape



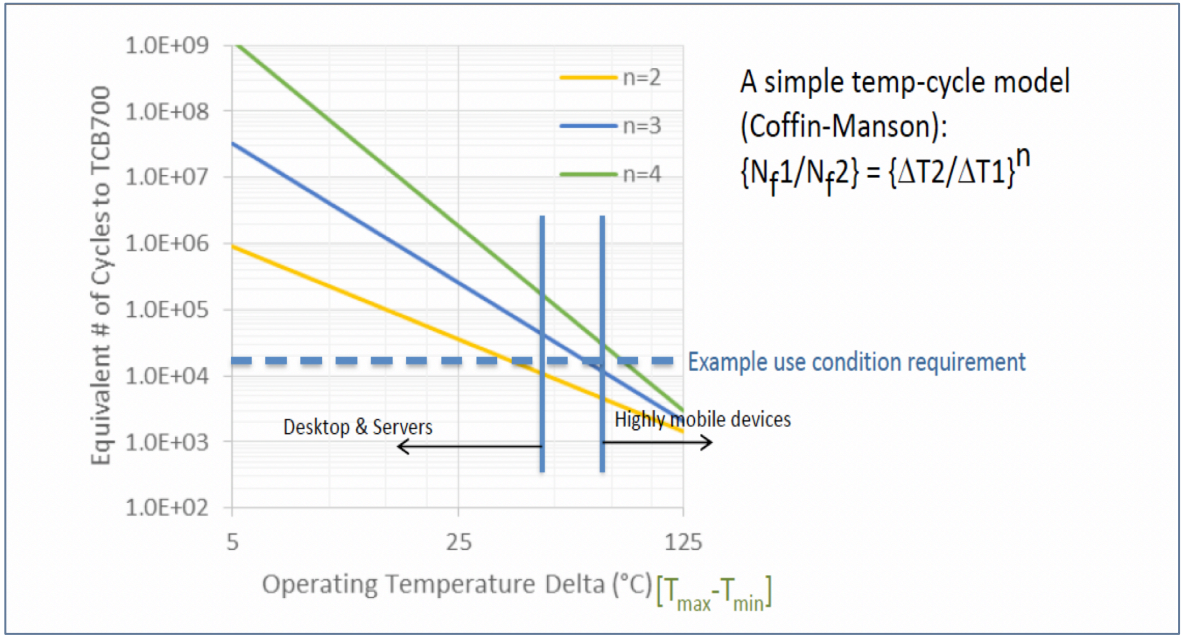
- Because of the custom/market specific nature of 2.5/3D packaging, mil-aero uses become custom/product specific as well.
- NASA EEE parts R&D work to focus Physics of Failure of materials sets/mechanical combinations
- Use this to provide guidance to projects
- Not a qualification solution however.
  - Mission and technology specific

Stress based Qualification Limitations



- Basic Arrhenius assumptions about 1000hr HTOL stress for acceptance
- Probability of failure conclusions are high for missions > 5 years in length
- System in Package technologies require new materials, construction and bias profile
- Qualification and reliability determination need investigation in failure methods
- Application specific qualification methods may be required for applications to space missions
- Having a phenomenological model of degradation is critical to 2.5D technology assessment

Coffin-Manson/Norris-Landzberg is the fundamental tool



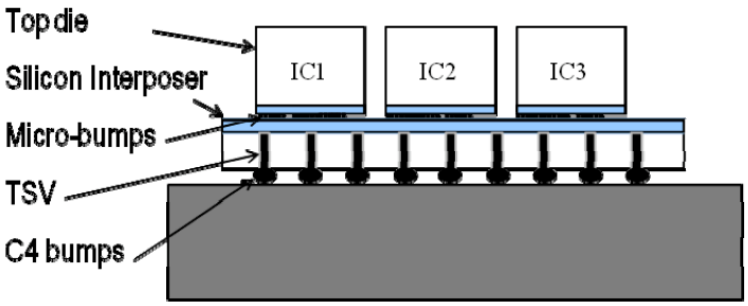
- Temperature cycling remains the fundamental method for evaluating packaging technologies
- The assumptions and predictions that are used can produce significant differences in final results
- Independent validation of mechanisms would be valuable for highly complex structures

Common Failure modes versus use conditions

	Reliability failure mechanism	Extreme use condition
1	Front end: **transistor gate di-electric** reliability	- **High power states** at high voltage, frequency, temperature and current e.g. Turbo mode
2	Backend: **Di-electric breakdown**	
3	Backend & bumps: **Electro-migration**	
4	Backend: **stress voiding**	- **Sustained operation** at high temperatures
5	**Moisture ingress:** De-lamination, electro-chemical corrosion, metal migration, pop-corning etc.	- **Low power modes like OFF/Stand-by** - **High humidity** and **temperature** ambient conditions e.g. 25C 80% RH
6	**Temperature cycling:** Cracking and de-lamination	- **Repeated cold temperature exposures** when part may be OFF - **Power cycles** when part is ON

- Dominant failure modes in servers, cell phones and wearables will be different because usage is different
- Commercial technologies must be evaluated in respect to the end market

Xilinx 20nm CoWoS



Overall package	Body size	55x55 mm
Top Chip	Chip size	3 slices Each 14x23 mm
	Pitch/Solder	40um/CuSnAg
TSV Interposer	Via diameter	10um
Organic substrate	Core thickness	1200um
	BGA pitch	1 mm
	Interposer Pitch/bump	180um/Eutectic

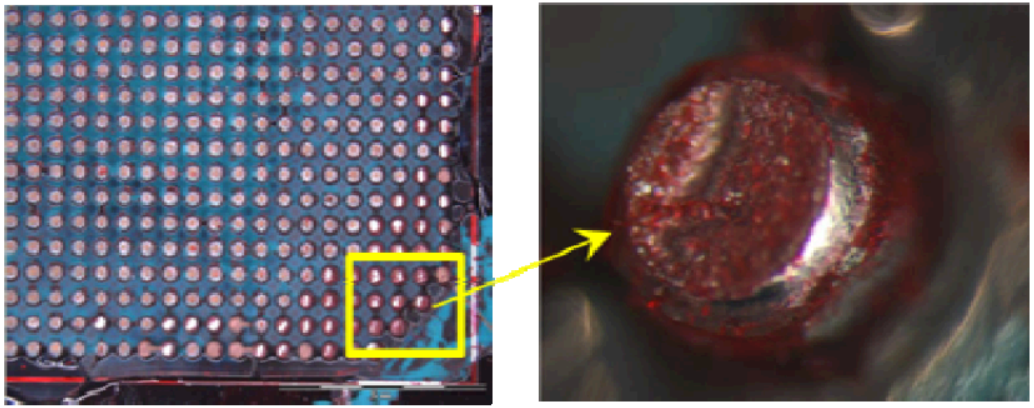
Materials	Young's modulus (GPa)	CTE (ppm)
Substrate core A	33	x,y =11 z =19
Substrate core B	23.6	x,y =7.7 z =12
Si	150	3
ubump UF	6.7	31
C4 UF	8.5	32
Copper	130	17
Solder mask	5.0	38
Sn Ag solder	51	22.4
TIM C	0.53e-3	71
Sealant C	3.3	28
TIM D	7.2e-3	200
Sealant D	7.2e-3	200
Eut solder	31.5	25.3

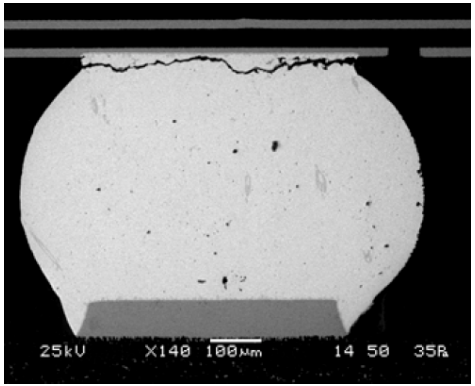
- "Extreme TSV interposer"
- Three 23x14mm die slices on a 25x45mm Si interposer w/ Cu through Silicon Via
- Low-k chip 375,000 micro bumps
- Interposer
  - 1000um thick
  - 55x55mm substrate
  - 30,000 C4 bumps
  - 2,982 BGA balls on substrate

Reliability Evaluation of an Extreme TSV Interposer and Interconnects for the 20nm Technology CoWoS IC Package, Banikamali, et. al ECTC (2015)

Xilinx 20nm CoWoS

- Need very high bump yield (micro, C4)
- Implemented proprietary test structure to test every bump
- Optimized process and design for high yield
- Significant use of thermo-mechanical materials modeling
  - Package warpage
  - Die stress during temperature exposure
  - Optimization of stress between materials
  - Energy Release Rates (ERR) fracture mechanics
- Board level reliability modeling
  - Strain, inelastic energy
- Board level reliability test (IPC-9710)
- Temp cycle (0-100C)
  - 1st fail at 1645 cycles
  - All fail after 2741 cycles
  - Solder ball crack at package corner ball
    - Not at C4 or micro bump

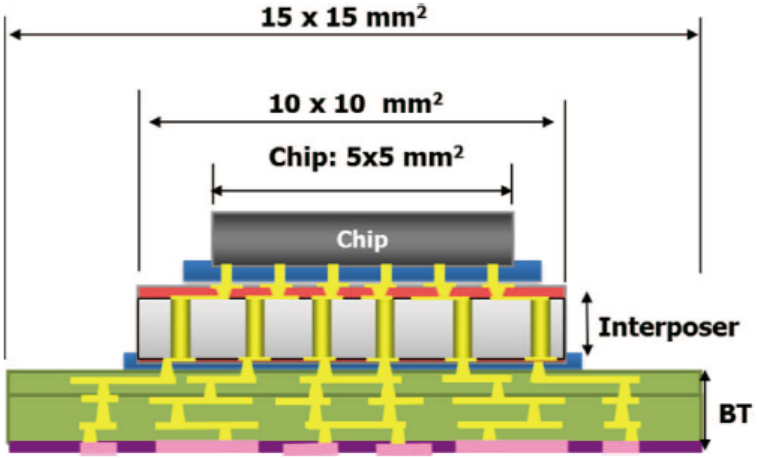




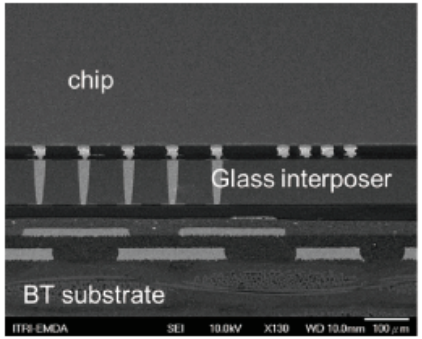
Silicon vs. Optical Interposer

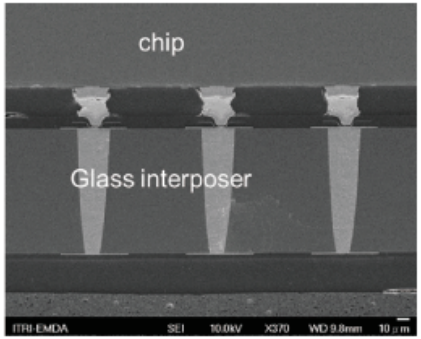
- Not a particularly good insulator or conductor
- CTE differences with Cu during TSV forming process
- Cost due to need for electrical insulation around via sidewall
- Wafer size can be limiting

- Electrical isolation
- Improved RF performance
- Improved CTE performance
- Low cost options



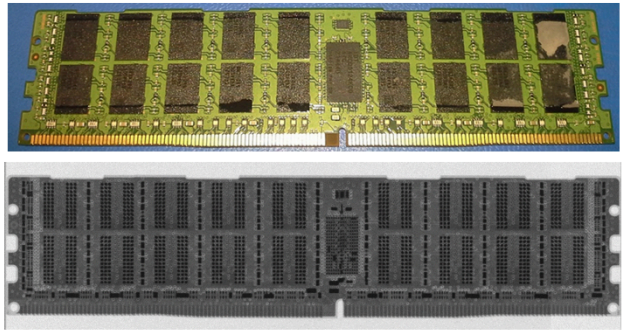
- 100um thick
- 100 & 150 um bump pitch
- 2 RDL front /1 RDL back
- -55C to 125C / 2000 cycles
  - No optical failures

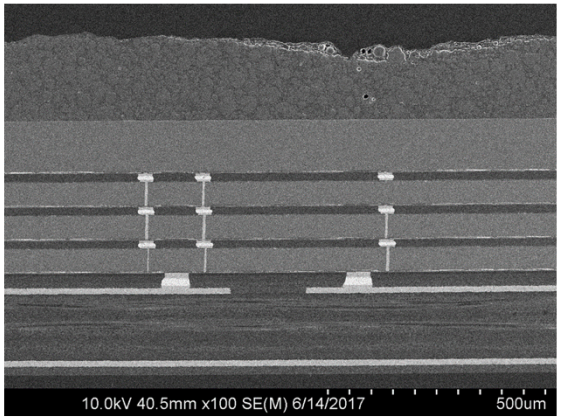


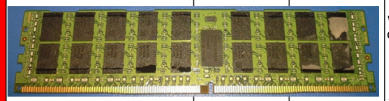


"Reliability Evaluation for Integrated Glass Interposer", CK. Lee, et. al, Japan Institute of Electronics Packaging, 2016

DDR4 TSV – NEPP Task

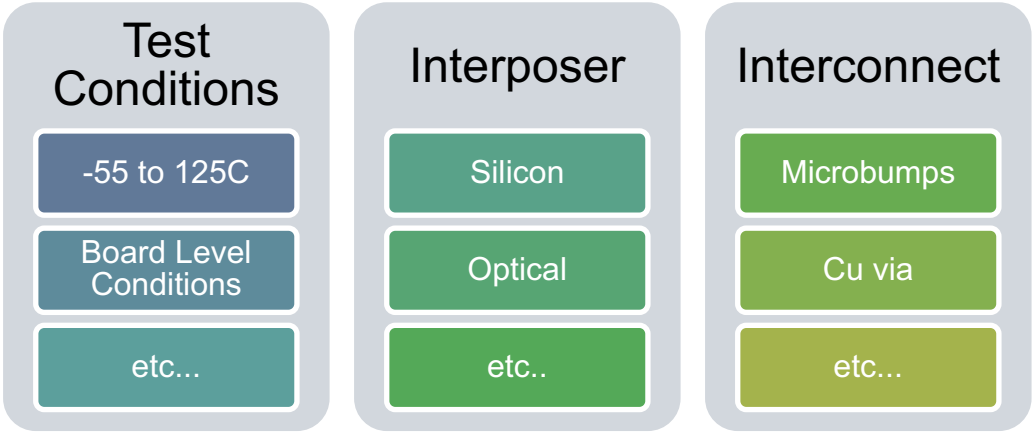




S/N	Condition	250 cyc	500 cyc	750 cyc	1000cyc	1250	
01	TC	Pass	Pass	Fail. Different failures at different voltages.			
02		Pass	Fail. Different failures at different voltages.				
03		Pass	Fail. Different failures at different voltages.				
04	125c 240 hr burn-in simulation + TC	Pass	failed Auto-ID (unable to read)				Suspected failure mode was SPD or RCD chip. SPD solder joint did not have crack. Did x-ray on RCD and found N]no issue. Did dye and pry on RCD and found no issue.
05		Pass	Pass	Fail. Different failures at different voltages.			
06		Pass	Pass	Pass	Pass	Fail. Different failures at different voltages.	
07	Underfilled BGA	Fail. Different failures at different voltages.	failed Auto-ID (unable to read)				
08		Pass	failed Auto-ID (unable to read)				

Jong-ook Suh and Joe Riendeau

Physics of Failure Database for 2.5/3D Technologies



- Current efforts are to focus on expanding failure and technology database

Summary

- 2.5/3D Technology continues to evolve rapidly
- Standard product vs custom products will remain an issue for determination of fitness of use
- Reliability evaluation still based on historical phenomenological modeling
- Successful mil-aero usage will require significant characterization and modeling throughout the entire manufacturing process and use conditions.

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